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| 10/564,236 | 01/10/2006 | Jose Solo De Zaldivar | DE03 0254 US1 | 6994 |

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| EXAMINER | |
|---|---|
| BOOKER, VICKI B | |
| **ART UNIT** | **PAPER NUMBER** |
| 2813 | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/564,236 | SOLO DE ZALDIVAR, JOSE | |
| | Examiner | Art Unit | |
| | Vicki B. Booker | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10 January 2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to the application filed January 10, 2006.

Currently, Claims 1-7 are pending.

### *Priority*

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 6 provides for the use of a metal bump, but, since the claim does not set forth any steps involved in the method/process, it is unclear what method/process applicant is intending to encompass. A claim is indefinite where it merely recites a use without any active, positive steps delimiting how this use is actually practiced.

Claim 6 is rejected under 35 U.S.C. 101 because the claimed recitation of a use, without setting forth any steps involved in the process, results in an improper definition of a process, i.e., results in a claim which is not a proper process claim under 35 U.S.C. 101. See for example *Ex parte Dunki*, 153 USPQ 678 (Bd.App. 1967) and *Clinical Products, Ltd.* v. *Brenner*, 255 F. Supp. 131, 149 USPQ 475 (D.D.C. 1966).

See also MPEP § 2173.05(q).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 6,232,563 B1; dated 05/15/2001) in view of Endo et al. (US 5,087,578; dated 02/11/1992).

Regarding Claim 1, Kim et al. disclose a method of fabricating a chip with an insulation layer for the side walls of metal bumps (FIG. 5A-5D; Column 2, paragraph 2 and Column 2, paragraph 4, line 8) with the chip comprising

-- a non-conductive chip's substrate 11,

-- metal pads 12 deposited on the non-conductive chip's substrate 11,

-- a passivation layer 13 covering the non-conductive chip's substrate 11 and the edges of the metal pads 12,

-- a metal diffusion stop barrier 14 covering a portion of the chip's passivation layer 13 and the metal pads 12,

-- a photo resist pattern 45 on a metal layer to expose portions of the metal layer on the pad that is removed after use (Column 4, paragraph 4, lines 1-3) and

-- at least one bump on the exposed portion of the pad 36 and the edges of the metal layer characterized by the steps of

-- depositing the metal layer covering the chip's passivation layer and the metal pads (Column 4, paragraph 3, lines 11-13; "barrier layer"; TiW/Au, Ti/Pd/Au),

-- depositing an insulation layer (Column 4, paragraph 5, lines 1-6),

-- removing predetermined portions of the insulation layer 18' (FIG. 5C and 5D; Column 4, paragraph 6, lines 1-4), and

-- partially removing the metal layer such that the remaining metal material forms the bump diffusion stop barrier 14 (Column 4, paragraph 4, lines 6-8).

Kim et al. do not teach or disclose, however, depositing the insulation layer in a plasma activated reactor, and removing the predetermined portions of the insulation layer by reactive ion etching.

Endo et al. teach, in the same field of endeavor (Column 1, paragraph 2), removing an insulation layer 18 from a metal bump electrode by reactive ion etching (FIG. 1A and 1B; Column 1, paragraph 6, lines 15-20).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the method of Kim et al. by using reactive ion etching to remove predetermined portions of the insulation layer on the metal bump as taught by Endo et al.

The motivation for doing so at the time of the invention would have been to pattern the insulation layer to form electrodes for external contact as taught by Endo et al. (See FIG. 1A – 1C and Column 1, paragraph 6, lines 15-25).

Also, it would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the method of Kim et al. in view of Edo et al. by using a plasma deposition, since Kim et al. teaches that the deposition can be by CVD (See Kim et al., Column 4, paragraph 5, lines 1-6), and the energy source for a CVD process can be plasma (See Van Zant, Page 372, Paragraph 2, lines 1 – 4). One of ordinary skill in the art would use a plasma deposition such as a plasma-enhanced CVD because of its ability to easily incorporate an in situ cleaning step prior to deposition (See Van Zant, Page 379, Paragraph 3).

Claims 2, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 6,232,563 B1; dated 05/15/2001).

Regarding Claim 2, Kim et al. disclose a connector for a chip's substrate 11 and an opposite substrate 22 (FIG. 6A and 6B; Column 2, paragraph 2; Column 5, paragraph 1, lines 3-6) comprising:

- a plurality of electrode pads 21 on the opposite substrate 22;
- a plurality of electrically conductive bumps 16' on the chip's substrate 11, each of the electrically conductive bumps 16' being electrically connected to a respective one of the plurality of electrode pads 21 on the opposite substrate 22;

- a plurality of conductive particles 19 on respective top surfaces of the electrically conductive bumps 16' electrically connecting respective electrically conductive bumps 16' to the plurality of electrode pads 21, and
- an insulating layer 18' formed of a nitrate or an oxide on the surfaces of the side walls of each of the plurality of electrically conductive bumps 16' to prevent an electrical short between two bumps characterized in that the insulation layer is provided by an CVD process (FIG. 5A - 5D; Column 4, paragraph 5, lines 1 – 6).

Kim et al. do not teach or disclose that the insulating layer 18' is formed by LPCVD.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the method of Kim et al. by using a LPCVD process, since LPCVD, as a species of CVD processing, is used for most films deposited for advanced circuits as taught by Van Zant, and has advantages of providing good step coverage and uniformity as taught by Van Zant (See Van Zant, "Microchip Fabrication – A Practical Guide to Semiconductor Processing", Page 372, Paragraph 5, lines 3-5; and Page 377, Paragraph 3).

Regarding Claim 6, Kim et al. disclose use of a metal bump 16' that is partially covered with an insulation layer 18' which is deposited by a CVD process (FIG. 5A - 5D; Column 4, paragraph 5, lines 1 – 6) for a Chip on Glass or a Chip on Foil packaging application (Column 1, paragraph 2; FIG. 6A and 6B; Column 4, paragraph 8 through Column 5, paragraph 1).

Kim et al. do not teach or disclose that the insulation layer 18' is deposited by LPCVD.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the method of Kim et al. by using a LPCVD process, since LPCVD, as a species of CVD processing, is used for most films deposited for advanced circuits as taught by Van Zant, and has advantages of providing good step coverage and uniformity as taught by Van Zant (See Van Zant, "Microchip Fabrication – A Practical Guide to Semiconductor Processing", Page 372, Paragraph 5, lines 3-5; and Page 377, Paragraph 3).

Regarding Claim 7, Kim et al. disclose an arrangement with a chip's substrate and an opposite substrate comprising:

- a plurality of electrode pads 21 on the opposite substrate 22;
- a plurality of electrically conductive bumps 16' on the chip's substrate 11, each of the electrically conductive bumps 16' being electrically connected to a respective one of the plurality of electrode pads 21 on the opposite substrate 22;
- a plurality of conductive particles 19 on respective top surfaces of the electrically conductive bumps 16' electrically connecting respective electrically conductive bumps 16' to the plurality of electrode pads 21, and
- an insulating layer 18' formed of a nitrate or an oxide on the surfaces of the side walls of each of the plurality of electrically conductive bumps 16' to prevent an electrical short between two bumps characterized in that the

insulation layer is provided by a CVD-process (FIG. 5A - 5D; Column 4, paragraph 5, lines 1 – 6).

Kim et al. do not teach or disclose that the insulation layer is provided by a LPCVD process.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the method of Kim et al. by using a LPCVD process, since LPCVD, as a species of CVD processing, is used for most films deposited for advanced circuits as taught by Van Zant, and has advantages of providing good step coverage and uniformity as taught by Van Zant (See Van Zant, "Microchip Fabrication – A Practical Guide to Semiconductor Processing", Page 372, Paragraph 5, lines 3-5; and Page 377, Paragraph 3).

Claims 3 – 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo et al. (US 5,087,578; dated 02/11/1992).

Regarding Claim 3, Endo et al. disclose metal bumps 16, 17 that comprise side walls that are covered with an insulation layer 18, 18a on at least two opposite side walls facing each other (FIG. 1A and 1B), characterized in that the insulation layer 18, 18a is a dielectric layer which is formed by CVD deposition (Column 1, paragraph 6, lines 15-16) and is partially etched back in an anisotropic plasma etcher (FIG. 1B; Column 1, paragraph 6, lines 17-20; reactive ion etching).

Endo et al. do not teach or disclose the insulation layer formed by a plasma deposition.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify the method of Edo et al. by using a plasma deposition, since the energy source for a CVD process can be plasma (See Van Zant, Page 372, Paragraph 2, lines 1 – 4) and plasma-enhanced CVD is advantageous in that an in situ cleaning step can be easily incorporated prior to deposition (See Van Zant, Page 379, Paragraph 3).

Regarding Claim 4, Endo et al. disclose metal bumps as claimed in Claim 3, characterized in that the dielectric material is selected from the group consisting of $SiO_2$ and $Si_3N_4$ (Column 1, paragraph 6, lines 15-16).

Regarding Claim 5, Endo et al. disclose metal bumps as claimed in Claim 3 characterized in that the metal bumps 32, 33 are formed of a noble metal or an oxidation resistant material such as gold (FIG. 2A; Column 3, paragraph 3, lines 1-2).

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vicki B. Booker whose telephone number is 571-270-1565. The examiner can normally be reached Monday through Thursday 9:30am to 6pm E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VBB
09/26/07

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